Attorney's Docket No.: 42P12752D

Patent

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Scot A. Kellar et al.

Serial No.: Not yet assigned

Filed: Herewith

For: WAFER BONDING FOR THREE-DIMENSIONAL (3D) INTEGRATION

Which is a Divisional of Application of:

Serial No: 10/066,643

Filed: February 6, 2002

Examiner: Not yet assigned

Art Unit: Not yet assigned

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

Applicant hereby requests consideration of the enclosed Information Disclosure Statement pursuant to 37 C.F.R §1.97(b). Attached is the PTO Form 1449 from the parent application filed on February 6, 2002 (Serial No. 10/066,643). These previous application is relied upon for an earlier filing date under 35 U.S.C. §120.

Pursuant to C.F.R. §1.98(d), copies of the references are not being provided herewith since they were previously sent to the Patent and Trademark Office. Please consider these cited documents in the currently pending §1.53(b) divisional application filed on February 6, 2002.

Pursuant to 37 C.F.R. § 1.97, the submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made and is not to be construed as an admission that the information cited in this statement is material to patentability.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 10/27, 2003

Michael A. Bernadicou
Reg. No. 34,935

12400 Wilshire Blvd.
Seventh Floor
Los Angeles, CA 90025-1026
(408) 720-8300

Form PTO-1449	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DKT. NO.	SERIAL NO.
		219.40605X00	10/066,643
		APPLICANT	
	INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)	Scot A. KELLAR et al.	
		FILING DATE	GROUP
		February 6, 2002	2811

U.S. PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
	AL						

FOREIGN PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Country	Class	Subclass	Translation	
							Yes	No
	AM							
	AN							
	AO							
	AP							
	AQ							
	AR							
	AS							
	AT							

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	AU	"Ultra Thin Electronics for Space Applications", 2001 Electronic Components and Technology Conference, 2001 IEEE
	AV	"Copper Wafer Bonding"; A. Fan, A. Rahman, and R. Reif; Electrochemical and Solid-State Letters, 2 (10) 534-536 (1999)
	AW	"Face to Face Wafer Bonding for 3D Chip Stack Fabrication to Shorten Wire Lengths", June 27-29, 2000 VMIC Conference 2000 IMIC – 200/00/0090(c)
	AX	"InterChip Via Technology for Vertical System Integration", Fraunhofer Institute for Reliability and Microintegration, Munich, Germany; Infineon Technologies AG, Munich, Germany; 2001 IEEE
	AY	
	AZ	

Examiner	Date Considered